REMARKS

Claims 1 – 35 are pending in the Application, of which claims 8-12 and 19-35 are withdrawn from consideration.

Specification Objection

The present Office Action alleges the title is not descriptive. Applicants have deleted the word "method" and changed the title to "A Flip Chip Semiconductor Die Internal Signal Access System" to reflect the withdrawal of the method claims 8 - 12 and 19 - 35.

Claim Objections.

Claim 5 is objected to because of an informality. Applicants respectfully assert Claim 5 does not have an informality and Claim 5 recitation "wherein said FIB pad is communicatively coupled" is appropriate.

102 Rejections

Claims 1 and 3 - 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Cheng et al. (US Patent No. 6,686,615). Applicants have reviewed the Cheng et al. reference and, for the following rationale, Applicants respectfully submit that the present invention is not anticipated nor rendered obvious by the Cheng et al. reference.

Applicants respectfully assert that the Cheng et al. reference is not directed to the present invention as recited in Claim 1. Specifically the present invention, as set forth in independent Claim 1 recites in part:

> ... said test signal redistribution trace is disposed such that multiple test signals are accessible at varying degrees of electronic component granularity ... .

To the extent the Cheng et al. reference may mention test connecting traces connecting with redistribution traces [Col. 3 lines 19 - 21], Applicants respectfully assert the Cheng et al. reference does not teach the conductive traces are disposed such that multiple test signals are accessible at varying degrees of electronic component granularity.

Applicants respectfully assert Claims 2 - 7 are allowable as depending from allowable independent Claim 1.

Claims 13, 14 and 18 are rejected under 35 U.S.C. 102 (b) as being anticipated by Lin (US Patent No. 5,258,648). Applicants have reviewed the Lin reference and, for the following rationale, Applicants respectfully submit that the present invention is not anticipated nor rendered obvious by the Lin reference.

Applicants respectfully assert that the Lin reference is not directed to the present invention as recited in Claim 13. Specifically the present invention, as set forth in independent Claim 13 recites in part:

> ...a conductive trace disposed such that multiple test signals are accessible at varying degrees of electronic component granularity... .

To the extent the Lin et al. reference may show a trace on Figure 5 and may mention an electrical connection between the test connection and via [Col. 7 lines 10 - 27], Applicants respectfully assert the Lin et al. reference does not teach the conductive traces are disposed such that multiple test signals are accessible at varying degrees of electronic component granularity.

Applicants respectfully assert Claims 14 – 18 are allowable as depending from allowable independent Claim 13.

103 Rejections

The present Office Action indicates Claim 2 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Cheng et al. in view of Lin. Applicants respectfully assert that the present invention is neither shown nor suggested by the Cheng et al. nor the Lin references, alone or together in combination.

Applicants respectfully reassert that the present invention as claimed in Claims 2 is neither shown nor suggested by the Cheng et al. reference and Claim 2 is allowable as depending from an allowable independent Claim 1 as argued above. The present Office Action acknowledges that the Cheng et al. reference fails to teach the conductive bump being electrically coupled to a test signal access component of a package substrate. Applicants respectfully assert that the Lin reference does not overcome these and other shortcomings of the Cheng et al. reference.

To the extent the Lin reference may show a trace on Figure 5 and may mention an electrical connection between the test connection and via [Col. 7

lines 10 - 27], Applicants respectfully assert the Lin et al. reference does not teach the conductive traces are disposed such that multiple test signals are accessible at varying degrees of electronic component granularity.

The present Office Action indicates Claims 15 -17 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Lin in view of Cheng et al. Applicants respectfully assert that the present invention is neither shown nor suggested by the Cheng et al. nor the Lin references, alone or together in combination.

With regards to Claims15-17 the present Office Action acknowledges the Lin reference fails to disclose a semiconductor die comprising a test signal redistribution layer comprising conductive traces; a test probe point for accessing signals in said semiconductor die and for electrical coupling to said test signal redistribution layer; a test access via for electrically coupling said test probe point to said test signal redistribution layer; and a conductive bump for conveying a test signal off of said semiconductor die to said package substrate, said conductive bump located on a first surface of said semiconductor die and electrically coupled to said test signal redistribution layer. The present Office Action also acknowledges the Lin reference further fails to disclose routing of

said test signal redistribution layer conductive traces is such that trace widths and spacing is a minimum without causing signal interference.

Applicants respectfully assert the Cheng et al. reference does not overcome these and other shortcomings of the Lin reference. As set forth above Applicants respectfully assert the Cheng et al. reference does not teach the conductive traces are disposed such that multiple test signals are accessible at varying degrees of electronic component granularity. The present Office Action alleges Cheng et al. appears to disclose in FIG 2 test signal redistribution layer conductive traces 21 are routed such that trace widths and spacing is a minimum without causing signal interference. To the extent the Cheng et al. reference may show traces [Figure 2] Applicants respectfully assert the Cheng et al. reference does not teach routing of test signal redistribution layer conductive traces is such that trace widths and spacing is a minimum without causing signal interference

CONCLUSION

In light of the above-listed amendments and remarks, Applicants respectfully request allowance of the remaining Claims. The examiner is urged to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

Wagner, Murabito & Hao

Date: 11/3/06

John F Ryan
Reg. No.: 47,050

Two North Market Street
Third Floor
San Jose, California 95113
(408) 938-9060